REMARKS/ARGUMENTS

Applicant has carefully reviewed and considered the Office Action mailed on October 11, 2007, and the references cited therewith.

Claims 1, 5, 16, 26, 33, 38, 47, and 55 are amended, claims 7, and 34-35 are canceled, claims 2, 12-15, 17-25, 36-37, 42-46, and 50-54 are withdrawn, and no claims are added; as a result, claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49, and 55-59 are now pending in this application.

§ 112 Rejection of the Claims

Applicant respectfully traverses the 112 rejections. Nonetheless, in the interest of furthering prosecution of the present case, the 112 claims are addressed as follows.

Claim 5 was rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement.

Claim 5 is currently amended so as to include additional features. Support for the amendment to claim 5 may be found in paragraph 0061 of the specification, as originally filed. Applicant respectfully submits that claim 5, as amended, complies with the written description requirement. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 112, first paragraph, rejection of claim 5.

Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

With respect to independent claims 1, 16, 26, 38, 47, and 55, regarding the rejection based on the Examiner's statement that the claims are "unclear as to which element is configured to inject current into the tunnel junction when the memory cell is selected", Applicant has endeavored to clarify the matter by amending the claims. For example, the last element of independent claim 1, as currently amended, presently recites, "each control element including a tunnel junction and a silicon-rich

insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected."

Among other locations in the specification as originally submitted, support for the amendment can be found in paragraph 0033, which recites, "The silicon-rich insulator 60 of the control element 45 injects current into the tunnel junction 70 of the control element when the memory cell 20 is selected".

Each of independent claims 16, 26, 38, 47, and 55 are currently amended consistent with the just-presented recitation of independent claim 1, as currently amended. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 112, second paragraph, rejection of independent claims 1, 16, 26, 38, 47 and 55, as well as those claims that depend therefrom.

Independent claims 47 and 55, as currently amended, are further amended to clarify the alignment aspects of the claimed structure. To note, the Office Action mailed October 11, 2007, indicated "memory cells of each set being at least partially aligned vertically with each other" as recited in claim 30. However, claim 30 does not recite such a limitation. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 112, second paragraph, rejection of independent claims 47 and 55, as well as those claims that depend therefrom.

As noted above, dependent claim 5 is currently amended so as to include additional features with respect to the tunnel junction element recited in independent claim 1. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 112, second paragraph, rejection of dependent claim 5.

§103 Rejection of the Claims

Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 as best understood were rejected under 35 USC § 103(a) as being unpatentable over Miyasaka (U.S. Patent No. 4,476,547) in view of Udayakumar et al. (U.S. Publ. No. 2005/0012126). Applicant respectfully traverses the rejection as follows.

Applicant does not admit that the Udayakumar reference is indeed prior art and reserves the right to swear behind at a later date. Nonetheless, in the interest of advancing prosecution thereof, Applicant respectfully submits that the claim elements of the application as currently presented are patentably distinguishable from the teachings of both the Udayakumar and the Miyasaka references.

Applicant's independent claim 1, as currently amended, presently recites:

> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

Applicant respectfully submits that the Miyasaka and Udayakumar references, individually or in combination, do not describe, teach, or suggest each and every element and limitation as recited in Applicant's independent claim 1, as currently amended.

On page 4 of the Office Action mailed October 11, 2007, the Examiner acknowledges, "Miyasaka does not teach that each control element including a tunnel junction and a silicon-rich oxide insulator." However, the Examiner suggests that the Udayakumar reference teaches the missing control element limitations, and further states, "It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a tunnel junction and a silicon-rich oxide insulator in each control element of Miyasaka's device in order to make an operable device and in order to improve the characteristics of the device, respectively."

Applicant respectfully submits that the suggested motivation to combine the Miyasaka and Udayakumar references (i.e., "in order to make an operable device and in order to improve the characteristics of the device") is overly conclusory and general because it potentially may be applied in an attempt to justify rejection of virtually any type of modification contemplated and, thus, does not provide motivation for making the specific modifications recited in the claims of the present application. As such, Applicant respectfully submits that a motivation to combine

has not been established and that a 103 rejection for obviousness is therefore inappropriate.

The Miyasaka reference appears to describe a memory cell pattern of a conventional 1-transistor-1-capacitor type dynamic RAM. (Col. 2, lines 40-42). From Applicant's review of the cited portions of the Miyasaka reference, Applicant respectfully submits that one having ordinary skill in the art would understand the capacitor of the Miyasaka device to conventionally perform a storage functionality and the transistor portion of the Miyasaka device to perform a control functionality of the memory cell described therein. As such, the Miyasaka reference does not appear to identify a storage element as a part of a control element, much less a silicon-rich insulator as forming part of a control element, as described in independent claim 1 of the present disclosure.

Applicant notes on page 10 of the Office Action, however, that the Examiner states, "Miyasaka teaches in figure 5 and related text a control element being a capacitor." Applicant respectfully submits that the capacitor portion of the "conventional 1-transistor-1-capacitor type dynamic RAM" device described in the Miyasaka reference does not describe, teach, or suggest a control element. Further, Applicant respectfully submits that the Miyasaka capacitor does not teach the claimed control element because one of ordinary skill in the relevant art would not then understand other features of the Miyasaka device as describing a storage element if the capacitor is taken as the control element rather than a storage element.

Applicant also respectfully submits that the Udayakumar reference does not teach, "each control element including a tunnel junction and a silicon-rich insulator", as recited in Applicant's independent claim 1, as currently amended. If the capacitor portion of the Miyasaka device indeed provides storage functionality to the memory cell described in Miyasaka reference, then additional features associated with a capacitor structure (e.g., storage element) in the Udayakumar reference, incorporated into the capacitor of the Miyasaka device, do not provide the missing control element claim limitations (i.e., "a tunnel junction and a silicon-rich oxide insulator", as recited in independent claim 1).

Applicant respectfully submits that it is inappropriate to identify the capacitor portion of the Miyasaka device (rather than the transistor portion) as being the control element. Applicant respectfully submits that the capacitor portion of the Miyasaka device is the storage element of the dynamic RAM device described in the Miyasaka reference and, thus, even if the Udayakumar reference teaches a tunnel junction and a silicon-rich oxide insulator associated with a capacitor, these features are directed at the storage portion of the Miyasaka device, not the control element, as recited in independent claim 1 of the present disclosure. Therefore, Applicant respectfully submits that, based upon the teachings of the Miyasaka reference, one of ordinary skill in the relevant art would not arrive at, "each control element including a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction", as recited in independent claim 1, as currently amended.

The Examiner states on page 4 of the Office Action that the Udayakumar reference teaches, "a memory cell Cfe having exactly two terminals and having a storage element and a control element wherein the control element including a tunnel junction and a silicon-rich oxide insulator SILOX2." However, Applicant submits that the Udayakumar reference does not teach "each control element including a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction", as recited in independent claim 1, as currently amended. As such, Applicant respectfully submits that the Miyasaka and Udayakumar references, individually or in combination, do not describe, teach, or suggest a tunnel junction and a silicon-rich oxide insulator, where the silicon-rich insulator injects current into the tunnel junction.

From Applicant's review, the Udayakumar reference does not describe a tunnel junction, nor injection of current into the tunnel junction, in particular from a silicon-rich insulator. That is, although the Udayakumar reference appears to describe a silicon-rich oxide insulator layer, the silicon-rich insulator layer does not appear to inject current into the tunnel junction. The Examiner does not identify

with particularity where in the Udayakumar reference this element is described, taught, or suggested.

The Udayakumar reference also appears to describe an AlOx layer. However, the AlOx and silicon-rich insulator layers appear to be used in the Udayakumar reference only as hydrogen barriers, not as a tunnel junction and silicon-rich oxide insulator configured to inject current into the tunnel junction. Neither layer appears to be included in a control element.

Instead, the Udayakumar reference appears to describe both layers being formed as a hydrogen barrier above a specific type of capacitor to prevent or mitigate degradation of the capacitor ferroelectric materials due to exposure to hydrogen in back-end processing in many CMOS integration schemes. (See paragraphs 0021 and 0023 of the Udayakumar reference). A first hydrogen barrier (e.g., AlOx) and a second hydrogen barrier (e.g., silicon-rich oxide insulator (SILOX)) appear to be formed over the ferroelectric capacitors for protection thereof. Hence, the Udayakumar reference appears to describe fabrication of a control element (e.g., a transistor) but does not appear to utilize a silicon-rich oxide insulator and/or a tunnel junction in formation of the control element. (See Figure 4A and related text).

The Examiner presents what appears to be an inherency argument based on an assumption that a silicon-rich oxide insulator injecting current into a tunnel junction is inherent in the capacitor stack structure described in the Udayakumar reference. However, the Udayakumar reference does not appear to describe, teach, or suggest a tunnel junction. Only Applicant's disclosure seems to address "a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction", as recited in independent claim 1, as currently amended.

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill in the relevant art. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of

circumstances is not sufficient. To rely upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics *necessarily* flows from the teachings of the applied prior art. In this instance, Applicant respectfully submits that a tunnel junction and a silicon-rich insulator, where the silicon-rich insulator injects current into the tunnel junction, need not be an essential element in implementing AlOx and silicon-rich insulator layers comprising a hydrogen barrier.

The Examiner suggests that the "prior art's" structure is identical to the claimed structure. Applicant respectfully submits that the thickness of a tunnel junction layer must be thin enough to allow tunneling of electrons. However, to function as a hydrogen barrier, the AlOx and silicon-rich insulator layers described in the Udayakumar reference are deposited as a relatively thick layer. The silicon-rich insulator layer of the Udayakumar reference is deposited to a thickness of about 300-500 Angstroms (see paragraph 0026), and AlOx is deposited to a thickness of about 100 Angstroms (see paragraph 0025).

The cited portions of the Udayakumar reference do not appear to describe, teach, or suggest that these relatively thick layers of AlOx and silicon-rich insulator are capable of functioning as "a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction", as recited in independent claim 1, as currently amended. Applicant respectfully submits that the relatively thick hydrogen barrier layers described in the Udayakumar reference are not identical to the claimed structure, and thus do not inherently possess the claimed limitations.

Applicant further submits that "a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction", as recited in independent claim 1, as currently amended, is not a recitation of intended use of the claimed invention, but rather defines a particular configuration of the silicon-rich insulator (and tunnel junction arrangement) included in the claimed structure. As discussed above, certain configurations and/or thicknesses of an AlOx layer may not be functional as a tunnel junction layer, and/or certain configurations (including

thicknesses) of a silicon-rich insulator layer may not be capable to inject current into the tunnel junction.

The Examiner states on page 4 of the Office Action that "each control element including a tunnel junction and a silicon-rich insulator configured to inject current into the tunnel junction when the memory cell is selected" includes features that are inherent due to the claimed structure being identical to structure described in the cited references. Applicant respectfully submits the structures described in the Miyasaka and Udayakumar references are not identical because they are not configured to produce the claimed functionality (e.g., "a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction", as recited in independent claim 1, as currently amended).

Moreover, the Examiner seems to consider the silicon-rich insulator that forms a portion of the control element (along with the tunnel junction) to be a capacitor (e.g., a storage element), as appears to be described in the Miyasaka and Udayakumar references. Applicant respectfully submits that the storage element and the control element of the present disclosure are distinct elements serving different functions. For example, independent claim 1, as currently amended, recites, "each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon-rich insulator". In addition, Figure 2 of the present application shows the storage element 50 to be separate and distinct from the silicon-rich insulator 60 that, in combination with the distinct tunnel junction 70, contributes to formation of the control element 45.

Applicant further notes that the specification of the present disclosure recites, "Silicon-rich insulator 60 may be considered an electronic switch that allows selection of the memory cell for programming and sensing the storage state, as well as isolation of the memory cell when the memory cell is unselected." (Paragraph 0034). Hence, Applicant respectfully submits that the silicon-rich insulator is not equivalent to a storage element (e.g., a capacitor) because the storage element is separate and distinct (e.g., see independent claim 1 and Figure 2) and that the

silicon-rich insulator does not function as a storage element (e.g., a capacitor) because the silicon-rich insulator forms part of the control element functioning as an electronic switch that allows selection of the memory cell for programming and sensing the storage state (e.g., of the storage element).

Applicant's independent claim 16, as currently amended, presently recites:

> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, each means for controlling including a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

Independent claim 26, as currently amended, presently recites:

> f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, a silicon-rich insulator, and a tunnel-junction layer in series relationship between the first and second conductive layers, whereby the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.

Independent claim 38, as currently amended, presently recites:

> i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.

Independent claim 47, as currently amended, presently recites:

> i) forming and patterning a second conductive layer over the tunnel-junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory

> cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

In addition, independent claim 55, as currently amended, presently recites:

> i) forming and patterning a second conductive layer over the storage-element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator current into the tunnel-junction layer when the memory cell is selected,

With particular regard to product-by-process independent claims 38, 47, and 55, Applicant respectively submits that the method steps produce a distinct structure not described, taught, or suggested by the Miyasaka and Udayakumar references, individually or in combination. Hence, Applicant respectfully submits that the resulting structure produced by the claimed method steps in independent claims 38, 47, and 55, as currently amended, is both novel and non-obvious over the cited references for the reasons set forth above.

As such, Applicant respectfully submits that the presently claimed invention is neither taught by, nor made obvious in view of, the combination of the Miyasaka and Udayakumar references. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 103 rejection of independent claims 1, 16, 26, 38, 47, and 55, as well as those claims that depend therefrom.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Thi Dang at (858) 655-8519 to facilitate prosecution of this matter.

At any time during the pendency of this application, please charge any additional fees or credit overpayment to the Deposit Account No. 08-2025.

CERTIFICATE UNDER 37 C.F.R. §1.8: The undersigned hereby certifies that this correspondence is being transmitted to the United States Patent Office facsimile number (571) 273-8300 on January 8, 2008

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